Finding the Hidden Field Sources in Switching Converters

High dv/dt Areas, High di/dt Loops, and Geometry Behind Converter Noise & Failures

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The schematic may be correct while the physical implementation is already creating its own failure path.

Fast switching does not only move energy through copper. It creates electric and magnetic fields around high dv/dt areas and high di/dt loops.

When those fields are not controlled, the result may appear as EMI, ringing, overshoot, control instability, false triggering, heating, semiconductor stress, or coupling into nearby circuits.

Many papers explain high di/dt loops and hidden electric-field coupling sources. **This paper presents a practical early design step: identify critical switching loops**, minimize copper areas that become field sources, recognize package structures that influence coupling, and control high-frequency return paths.

The goal is not only to reduce noise. It is to recognize these paths early enough that layout, part selection, thermal management, control stability, and mitigation choices remain available.

> **Converter problems often begin as geometry problems.**
>
> Find the high dv/dt areas, the high di/dt loops, and the structures that allow those fields to couple.

Addressed late, these problems are harder to fix. Early choices — copper area, package selection, return paths, mechanical placement, and heatsinking — can become constraints once the layout and assembly are fixed.

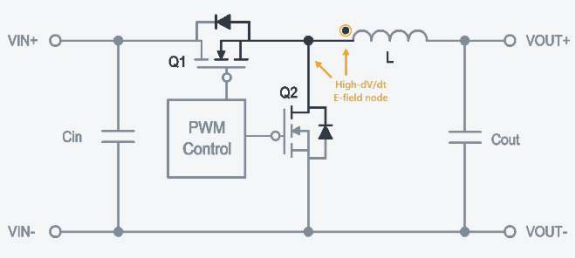
Some risks stay hidden until real switching stress appears. A FET may look correct on the datasheet, yet still see overshoot, gate disturbance, heating, or repeated stress when geometry lets fields form and couple unintentionally.

> **The schematic is complete. The converter is physical.**
>
> Layout, part selection, packaging, and supporting devices introduce parasitic elements the schematic does not show.

Identifying the E-Field Node(s)

Electric fields, or e-fields, exist between conductors at different voltages. In switching converters, the most important e-field coupling sources are usually the nodes whose voltage changes quickly.

A simple way to find them is to compare each schematic node during each switching state. For a buck converter, when Q1 is on, the switch node between Q1, Q2, and L is pulled toward VIN. When Q2 is on, that same node is pulled toward ground.



The input and output capacitors ideally remain at relatively constant voltage, so they usually drop out of this first-pass high dv/dt review.

The switch node becomes the primary e-field concern because physical copper, package structure, or connected conductors are driven through a large voltage change in a very short time. The switching frequency defines how often the event occurs; the transistor edge rate drives the high-frequency coupling.

E-field areas should be kept as small as practical to reduce coupling risk.

A MOSFET drain tab or switch-node tab is a common example. Connecting it directly to a heatsink may be thermally convenient, but it can greatly increase the effective dv/dt area. The heatsink can become part of the e-field coupling structure, turning a small switch-node area into a much larger coupling source.

Inductor construction can also matter. Even when a part has a high self-resonant frequency, winding structure, shielding, orientation, and placement can affect how the switch-node field couples into or through the component.

Inductors are often treated as non-polarized, but internal winding construction and placement can affect switch-node E-field coupling and EMI behavior.

Orientation Impact — Estimated EMI Peak Increase[1]

Frequency	Increase
360 kHz	+15 dB
720 kHz	+14 dB
25 MHz	+10–11 dB
85 MHz	+11 dB
400 MHz	+3 dB

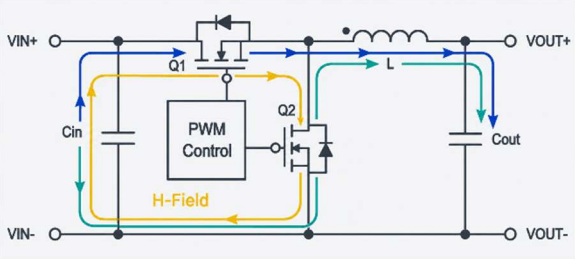
[1] Approximate values estimated from a re-digitized source plot.

Identifying the H-Field Loop(s)

Magnetic fields, or H-fields, are created where current changes. In switching converters, the most important H-field sources are usually the physical loops where current changes rapidly during each switching transition.

The identification method is similar to the E-field review: consider one conducting device at a time and map the current path.

For a buck converter, when Q1 is on, current shown in blue flows from Cin, through Q1, through L, through the output path, and back toward the input return. When Q2 is on, current shown in green freewheels through Q2, through L, and through the output path.



The important H-field loop is found by comparing those two paths. The section of the circuit that changes between Q1 conduction and Q2 conduction is the high di/dt loop. In a synchronous buck converter, this loop (shown in gold) is typically formed by Cin, Q1, Q2, and the return path back to Cin.

This loop is highly sensitive to placement. Traces, vias, package leads, and copper geometry all add parasitic inductance that is not shown in the schematic. The goal is to place Cin, Q1, and Q2 close together, minimize the enclosed loop area, keep connections short, and use low-inductance copper paths without unnecessarily increasing high dv/dt copper area.

This becomes especially important with fast devices such as silicon carbide, SiC, and gallium nitride, GaN, transistors. Faster edge rates can make even a few nanohenries of loop inductance create voltage overshoot, ringing, and repeated semiconductor stress.(2)

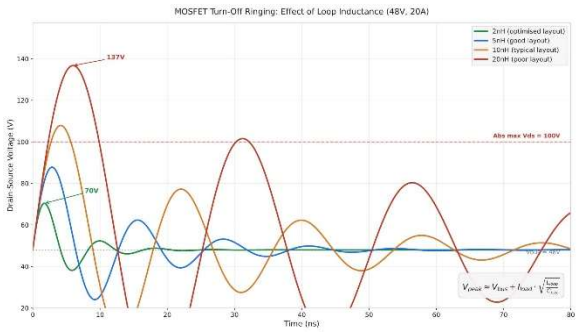


Figure 1 - Effect of loop inductance on FET stress *(2)*

The schematic shows the intended current path. The layout determines the magnetic-field loop.

> **Schematic shows intent.**
> **Layout defines the field loop.**

Other Topologies

This same identification technique can be applied to most power-converter layouts. The basic approach remains the same: review the design one switch state at a time, identify the nodes whose voltage changes quickly, identify the loops whose current changes quickly, and map the physical structures involved.

Buck, boost, buck-boost, half-bridge, full-bridge, flyback, and forward converters all create field sources through the same basic mechanisms. High dv/dt areas create electric-field coupling risk. High di/dt loops create magnetic-field coupling risk. The topology mainly changes which components are involved and where those areas and loops appear.

Resonant converters may require extra care. In LLC, phase-shifted full bridge, and similar designs, the review must account for control phase, dead time, tank current direction, and natural versus driven conduction to determine where voltage and current transitions actually occur.

In all cases, the practical question remains the same:

Which physical areas see fast voltage change, and which physical loops carry fast-changing current?

When Coupling Becomes EMI

An electric field by itself is not always a radiating EMI problem. The concern grows when a fast-changing voltage drives displacement current into nearby metal, planes, heatsinks, shields, or enclosure structures.

That current must return somewhere. If the coupling path becomes large enough, the system now has both electric-field and magnetic-field behavior. It may become a common-mode current path, a larger loop, or a structure that radiates more effectively.

The same is true for H-field coupling. A high di/dt loop creates a magnetic field that can induce current in nearby loops, planes, cables, shields, or control circuits. If those induced currents spread into larger structures, the original local switching loop can become a system-level EMI source.

This is why grounded metal, such as a heatsink near a high dv/dt node, is not automatically a shield. The same structure that appears to contain the field can also become a return path for displacement current, increasing high-frequency current into chassis, safety ground, nearby circuits, or cables.

The key question is not whether metal is grounded. It is what current the grounding path allows to flow, and where that current returns.

Summary: Identify Before You Mitigate

Converter EMI, ringing, instability, heating, and semiconductor stress often begin with the same practical question:

Where are the fast-changing fields being created, and where can they couple?

For high dv/dt effects, identify the nodes whose voltage changes quickly, then minimize the copper, package exposure, heatsink coupling, and nearby conductive structures attached to those nodes.

For high di/dt effects, map each switching state, compare the current paths, and keep the changing loop area short, tight, and low inductance.

This process does not replace filters, snubbers, shielding, or gate-drive tuning. It makes those choices more effective by first identifying the physical source of the problem.

Practical review checklist

- Before layout: identify the high dv/dt node(s), map each switching state to find the high di/dt loop(s), and try alternate placement options before routing
- Minimize switch-node area and high di/dt loop area.
- Control return paths **before** adding mitigation.
- Treat heatsinks, shields, planes, and enclosures as possible coupling paths.
- Test inductor orientation for impact on EMI and field coupling.

Remember that fast SiC and GaN devices magnify layout mistakes.

> **Schematic shows intent.**
> **Layout defines field behavior.**

References cited in this Insight (with permission of owners):

[1] **Data estimate derived from:** "Does the Assembly Orientation of an SMPS Inductor Affect Emissions?" *Analog Dialogue*, Analog Devices, Vol. 55, No. 2, June 2021.

[2] PCB Layout for Switchmode Converters: The Loops That Determine Whether Your Design Works Philip Bassett, June 2026, https://switchmode.io/

Additional resource related to SiC devices:

Mitigating EMI with SiC Solutions in Renewable Energy and Grid-Connected Power Converters, Wolfspeed, PRD-08907